

A Novel Design Methodology for High-Efficiency Current-Mode and Voltage-Mode Class-E Power Amplifiers in Wireless Power Transfer systems

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Abstract—The high-efficiency current-mode (CM) and voltage-mode (VM) Class-E power amplifiers (PAs) for MHz wireless power transfer (WPT) systems are first proposed in this paper and the design methodology for them is presented. The CM/VM Class-E PA is able to deliver the increasing/decreasing power with the increasing load and the efficiency maintains high even when the load varies in a wide range. The high efficiency and certain operation mode are realized by introducing an impedance transformation network with fixed components. The efficiency, output power, circuit tolerance, and robustness are all taken into consideration in the design procedure, which makes the CM and the VM Class-E PAs especially practical and efficient to real WPT systems. 6.78 MHz WPT systems with the CM and the VM Class-E PAs are fabricated and compared to that with the classical Class-E PA. The measurement results show that the output power is proportional to the load for the CM Class-E PA and is inversely proportional to the load for the VM Class-E PA. The efficiency for them maintains high, over 83%, when the load of PA varies from 10 to 100 Ω , while the efficiency of the classical Class-E is about 60% in the worst case. The experiment results validate the feasibility of the proposed design methodology and show that the CM and the VM Class-E PAs present superior performance in WPT systems compared to the traditional Class-E PA.

Index Terms—Wireless power transfer (WPT), current-mode (CM) Class-E power amplifier (PA), voltage-mode (VM) Class-E PA, high-efficiency, load-pull analysis, impedance transformation network.

I. INTRODUCTION

WIRELESS charging technology for portable electric devices has received intensive attention and realized commercialization by the lunch of Qi standard [1], [2]. It makes the power transfer more flexible and provides a comfortable user experience. This technology has been constantly improving and lots of efforts have been paid to pursue larger charging freedom, higher efficiency, and better performance for concurrent multiple charging (a technique that transmits

power concurrently to multiple receiving coils) [3]–[8]. However, most of them have been focusing on the coupling coils and research on the high-frequency high-efficiency power source for wireless power transfer (WPT) is lacked [6]–[11].

The majority of power sources that have been used in WPT systems are inverters [12], [13]. They require at least four switches and usually work at tens to hundreds of kilohertz (KHz). For the requirements of smaller circuit size and larger charging freedom, a new operating frequency 6.78 MHz for WPT has received more and more attention [14], [15]. It belongs to the ISM band and has been adopted by Rezenze standard proposed by the Alliance for Wireless Power (A4WP). The switch loss of inverters become considerably large at this frequency and thus a high-performance power source working at 6.78 MHz is required. The power source should maintain a high efficiency under the dynamic charging environment, i.e., the misalignment of coil coupling and the change of number of charging devices [16], [17]. Besides, it is expected that the power source is able to work in a certain mode, i.e., work as a current source or a voltage source [18], [19], for which the relationship of the output power and the load is predetermined. The power source with a certain operation mode is especially valuable to concurrent multiple charging systems, where the output power of source should adapt to the power requirements of charging devices. For instance, the load of power source in [16] increases as the number of charging device goes up, which indicates that the power source in this system should work as a current source, providing increasing output power with increasing load.

The Class-E power amplifier (PA) is a good candidate for MHz WPT systems due to its simple topology and high efficiency [20]–[22]. It is designed under zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions, which result in a 100% efficiency theoretically [23], [24]. The achievable efficiencies of the Class-E PAs are known to be about 90% when they operate at several to tens of MHz and deliver power of several to tens of watts [21], [25]. However, the ZVS and ZVDS conditions make the Class-E PA sensitive to the load variation, which is inevitable in real WPT systems due to the misalignment of coil coupling and the change of the number of receivers [16], [17]. The efficiency drops quickly when the load of PA deviates from the optimum value [26]. Besides, the traditional Class-E PA is neither a current source nor a voltage source and it can not ensure that the output power increasing or decreasing automatically as

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the load of PA increases [26]. Above all, the conventional design for Class-E PA can not meet the requirements of high-performance WPT systems and it has to be improved to satisfy the efficiency and power requirements simultaneously.

Some solutions have been proposed to solve the problem of efficiency reduction and power controlling. The parameters of Class-E PA, including frequency, duty ratio, capacitors, and inductors, are tuned to take the Class-E PA back to optimum working conditions and improve the efficiency [27]–[31]. The output power can be controlled by tuning the DC supply of PA. The method of tuning is straightforward and effective, but requires additional tuning, tracking, and control circuits, inevitably increasing the system scale and complexity. In this paper, the improved Class-E PA with simple topology and fixed components is used to obtain the high efficiency and certain operation mode through the method of impedance transformation. Here, the high-efficiency current-mode (CM) and voltage-mode (VM) Class-E PAs are first proposed and the design methodology for them is presented. The CM/VM Class-E PA is able to deliver the increasing/decreasing power with the increasing load and the efficiency of them maintains high even when the load varies in a wide range. The target power level of the PAs ranges from several to tens of watts, which are suitable for the application in electronic devices such as cellphones, wearable devices, laptops, and medical implant devices. The design methodology makes full use of load-pull and impedance transformation techniques. In the design flow, the target loads for PA are first defined according to the load-pull analysis. And then, a Π impedance transformation network is added into the circuit and a one-to-one mapping of PA's load and targeted value is established. The efficiency, operation mode, and circuit tolerance are all taken into consideration in the selection of target value, while these three criteria are seldom taken into account simultaneously in other's work. It makes sure that the PA is able to work efficiently and safely. All the circuit parameters are fixed and no controlling unit is used. Therefore, the circuit complexity and cost are greatly reduced, comparing to the system using tuning method. What's more, the robustness against random error for the impedance transformation is checked and a modified network is applied if necessary. It is valuable in the manufacture and makes the PA more practical in real systems. It is believed that the high-efficiency CM and VM Class-E PAs are promising for high-frequency high-efficiency WPT applications, especially for concurrent multiple charging systems.

II. ANALYSIS OF CLASS-E POWER AMPLIFIER

Fig. 1(a) shows the typical configuration of a Class-E power amplifier (PA). The MOSFET works as a switch and a square signal with 50% duty cycle is used to drive the PA. The DC power P_{DC} is injected into the circuit through a radio frequency (RF) choke L_f . The output power is P_0 and the efficiency of PA is defined as the ratio of P_0 to P_{DC} . L_0 and C_0 are designed to be resonant at the operation frequency, i.e., 6.78 MHz here. The values of the shunt capacitor C_S , residual reactance jX , and load R_l are specifically designed to maximize the efficiency of PA. Note that the design of the classical Class-E PA has been well documented in [23], [24].

TABLE I
CIRCUIT PARAMETERS IN SIMULATION.

V_{DD} (V)	L_f (μ H)	C_S (pF)	L_0 (μ H)	C_0 (pF)	X (Ω)
20	10	215	4.69	117.4	23

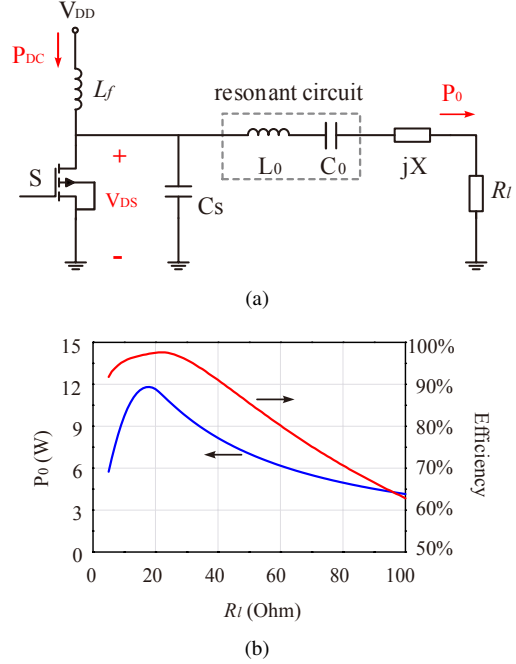


Fig. 1. The typical configuration and output performance of a Class-E power amplifier (PA). (a) The configuration of the Class-E PA. (b) The output power P_0 and efficiency of the Class-E PA versus the load R_l .

A well-known RF simulation tool, advanced design system (ADS) from Agilent, currently Keysight Technologies, is used to predict the performances of the PAs when working at MHz. The Pspice model of SUD06N10 (MOSFET) is applied in the simulation. The circuit parameters are listed in Table I. Fig. 1(b) shows the output performance of the PA when R_l is swept from 5 to 100 Ω . The efficiency achieves the highest value 97.6% when $R_l = 22 \Omega$ and decreases quickly when R_l deviates from this optimum value. The output power increases at first as R_l increases and then drops.

The Class-E PA is further analyzed by a load-pull simulation to take a deeper insight into the characteristics of the Class-E PA. The results are illustrated in Fig. 2. There are three groups of contours on the Smith chart, i.e., the constant output power contours, the constant efficiency contours, and constant contours for the peak value of MOSFET's drain voltage V_{DS_peak} . The power and efficiency contours provide an overview of the PA's output performance. The V_{DS_peak} contours show the region where the MOSFET is easy to be damaged. The points representing R_l varying from 5 to 100 Ω compose a load variation line, as is shown in Fig. 2. It goes through the high power region and extends to the low power area. Only a section of it locates within the high-efficiency region. These results are consistent with that shown in Fig. 1(b).

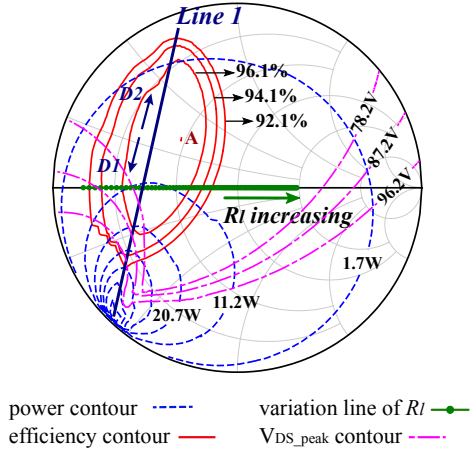


Fig. 2. The load-pull results of the classical Class-E PA.

Fig. 2 indicates that the output power P_0 , the efficiency, and the peak value of drain voltage V_{DS_peak} are absolutely determined by the impedance of PA's load. There is a large region on the Smith chart where the PA is able to achieve high efficiency in addition to the optimum point A. Therefore, the Class-E PAs do not have to be set under ZVS and ZVDS conditions to pursue the optimum efficiency. The Class-E PA can work efficiently if only all the loads lie within the high-efficiency area. What's more, the output power of Class-E PA versus load can be predetermined if the load varies in a certain way on the Smith Chart. The PA is able to deliver increasing power monotonically if the load increases along the direction in which P_0 increases, as the direction $D1$ shown in Fig. 2. The PA is able to produce reducing power monotonically if the load increase along the direction in which P_0 decreases, like the direction $D2$ shown in Fig. 2.

Thus, a high-efficiency Class-E PA with predetermined output power can be achieved by transforming the loads to the expected positions through an impedance transformation network. The circuit with an impedance transformation network is depicted in Fig. 3. The input impedance of the network Z_{in} is the equivalent load of the original Class-E PA. In this paper, two new types of Class-E PA based on this topology are proposed and built: the high-efficiency current-mode (CM) and voltage-mode (VM) Class-E PAs. The output power is proportional to the resistive load for the CM Class-E PA and is inversely proportional to the resistive load for the VM Class-E PA. The efficiency maintains high even when the load varies in a wide range. The design methodology for them is fully described in the next section.

III. DESIGN METHODOLOGY FOR THE HIGH-EFFICIENCY CM AND VM CLASS-E PAs

The design methodology for the high-efficiency CM and VM Class-E PAs is based on the load-pull and impedance transformation techniques. The output power, the efficiency, and the circuit tolerance are all taken into consideration in the design process. Besides, the robustness against the random error of the value of network components is also taken into account to further enhance the PA's performance. The design

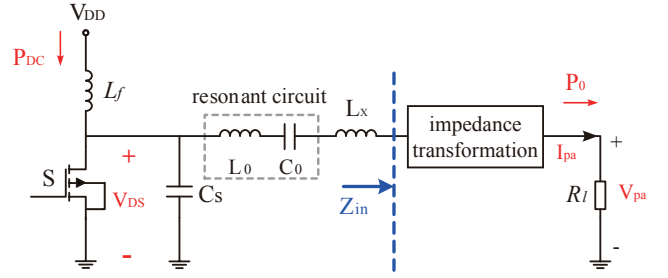


Fig. 3. The Class-E PA with an impedance transformation network.

flow for the high-efficiency CM and VM Class-E PAs is: 1) determine the target positions where the loads should be transformed; 2) build the impedance transformation network; 3) verify the robustness of the PA's performance and modify the impedance transformation network if it is necessary.

A. Location of Target Positions

The target positions where R_l should be transformed are located initially through placing a reference line $Line1$. Fig. 4 shows the reference lines for three different Class-E PAs, i.e., PA1, PA2, and PA3. The circuit parameters for these three Class-E PAs are the same to the previous settings in section II expect for C_S . C_S of PA1, PA2, and PA3 are 120, 215, and 330 pF, respectively. The reference lines lie within the high-efficiency region and intersect with each power contour only once to maintain a high efficiency and monotonicity of output power versus load. Considering that the largest drain voltage that SUD06N10 can withstand is 100 V, a margin of 10 V for the maximum V_{DS_peak} is left at least to protect the MOSFET. Thus, $Line1$ is placed within the V_{DS_peak} contour of 90 V. The reference lines are important and will be used in section III-B to design the impedance transformation network.

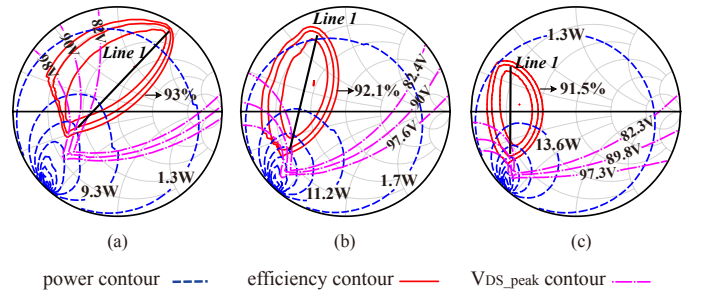


Fig. 4. The reference lines for three different Class-E PAs. (a) PA1. (b) PA2. (c) PA3.

B. Impedance Transformation Network

Here, a Π impedance transformation network is used, as is illustrated in Fig. 5(a), to transform R_l to the targeted positions. Z_{in} is determined by X_1 , X_2 , X_3 and R_l , as is shown in equation (1). It is transformed into the reflection coefficient given in equation (2) in order to match the Smith chart we use. Z_0 is the characteristic impedance of system, which is 50 Ω . The real and image parts of Γ_Z are functions

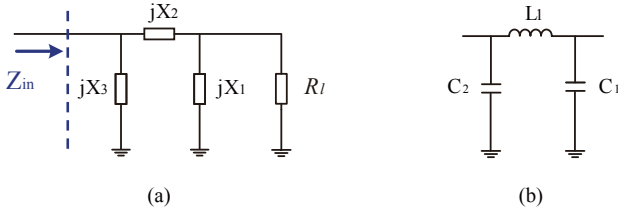


Fig. 5. The impedance transformation network. (a) The topology of the II impedance transformation network. (b) The real network in the system.

of X_1 , X_2 , X_3 and R_l . All the Z_{in} compose a load variation line on the Smith chart when R_l is swept from 5 to 100 Ω , as is shown in Fig. 6 and Fig. 8.

$$Z_{in} = \frac{jX_3 R_l (X_1 + X_2) - X_1 X_2 X_3}{R_l (X_1 + X_2 + X_3) + jX_1 (X_2 + X_3)} \quad (1)$$

$$\begin{cases} \Gamma_Z = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \\ f_1(X_1, X_2, X_3, R_l) = \text{real}(\Gamma_Z) \\ f_2(X_1, X_2, X_3, R_l) = \text{imag}(\Gamma_Z) \end{cases} \quad (2)$$

The target of the network design is to determine X_1 , X_2 and X_3 to make sure that the load variation line of Z_{in} matches the reference line *Line1* defined in section III-A as much as possible. *Line1* can be expressed as (3), where k , b , m , and n are constants and obtained directly from Fig. 4. Then the problem becomes: optimize X_1 , X_2 and X_3 to satisfy (4) and (5) with conditions (6)&(8) or (7)&(8). The operation mode is CM when the conditions (6)&(8) are applied and the operation mode is VM when the conditions (7)&(8) are used.

$$\Gamma_i = k \cdot \Gamma_r + b, \quad \Gamma_r \in (m, n) \quad (3)$$

$$k \cdot f_1(X_1, X_2, X_3, R_l) + b \rightarrow f_2(X_1, X_2, X_3, R_l), \quad (4)$$

$$f_1(X_1, X_2, X_3, R_l) \in (m, n) \text{ for any } R_l \in (5, 100). \quad (5)$$

$$f_2(X_1, X_2, X_3, R_{l1}) > f_2(X_1, X_2, X_3, R_{l2}) \text{ for } R_{l1} < R_{l2}. \quad (6)$$

$$f_2(X_1, X_2, X_3, R_{l1}) > f_2(X_1, X_2, X_3, R_{l2}) \text{ for } R_{l1} > R_{l2}. \quad (7)$$

$$X_1 < 0, \quad X_2 > 0, \quad X_3 < 0. \quad (8)$$

Among these equations (4) to (8), (4) and (5) ensure the alignment of the load variation line of Z_{in} and *Line1*; (6) and (7) ensure the monotonicity of output power versus load and decide the output mode; (8) makes sure that the shunt components are capacitors and the series component is inductor, as shown in Fig. 5(b), facilitating bypassing the harmonic power and improving the system's performance. This optimization problem can be solved by numerical method, such as exhaustive method and genetic algorithm. The solution provides initial values for X_1 , X_2 and X_3 and they can be further tuned manually in the simulation to get better performance.

1) *High-efficiency CM Class-E PA*: In order to validate the feasibility of the network structure and the algorithm, the impedance transformation networks *NC1* – *NC3* for PA1 - PA3 are designed, respectively. The CM Class-E PAs are then achieved by cascading the classical PAs to their corresponding network. Table II lists the value of components for each impedance transformation network.

TABLE II
DESIGN PARAMETERS FOR THE IMPEDANCE TRANSFORMATION NETWORKS NC1 - NC3.

	C_1 (pF)	L_1 (nH)	C_2 (pF)
<i>NC1</i>	408	997	278
<i>NC2</i>	510	530	360
<i>NC3</i>	668	309	237

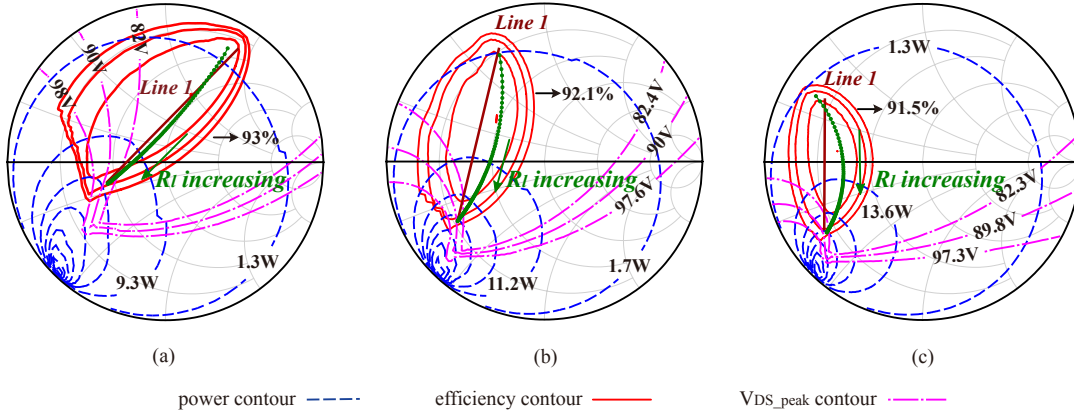
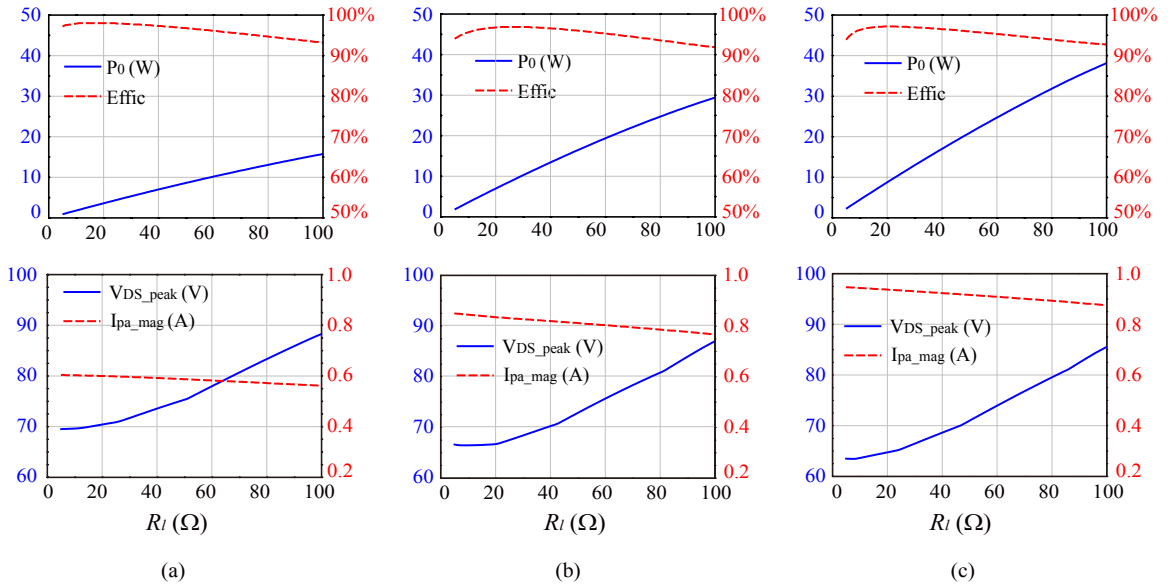
R_l is swept from 5 to 100 Ω and the corresponding Z_{in} is shown in Fig. 6. The load variation line of Z_{in} does not fully coincide with the reference line *Line1*. However, it is sufficient to achieve our objectives. The output performance of each CM Class-E PA is shown in Fig. 7. The efficiency keeps high when R_l varies and the output power P_0 is proportional to R_l . The magnitude of the PA's output current I_{pa_mag} decreases slightly as R_l increases. It can be observed that the PA with larger C_S produce higher I_{pa_mag} and P_0 . The V_{DS_peak} increases with increasing R_l and keeps under 90 V. All of them satisfy the targets we have set for the CM Class-E PA. It has to be mentioned that the method we use to derive the value of network's parameter can only ensure the monotonicity of output power versus load, but not the linearity. The linearity can be improved by properly tuning the network parameters, which is a process of trial and errors.

2) *High-efficiency VM Class-E PA*: In order to validate the feasibility of the network structure and the algorithm, the impedance transformation networks *NV1* – *NV3* for PA1 - PA3 are designed, respectively. The VM Class-E PAs are then achieved by cascading the classical PAs to their corresponding network. Table III lists the component's value for each impedance transformation network.

TABLE III
DESIGN PARAMETERS FOR THE IMPEDANCE TRANSFORMATION NETWORKS NV1 - NV3.

	C_1 (pF)	L_1 (nH)	C_2 (pF)
<i>NV1</i>	13245	121.4	6622
<i>NV2</i>	5337	218.4	4092
<i>NV3</i>	2897	303.5	3209

R_l is swept from 5 to 100 Ω and the corresponding Z_{in} is shown in Fig. 8. The load variation lines of Z_{in} for the VM Class-E PAs are similar to those of the CM PAs, but vary in the contrary direction. Fig. 9 shows the output performance of each VM Class-E PA. The efficiency keeps high when R_l varies and the output power P_0 is inversely proportional to R_l . The magnitude of the PA's output voltage V_{pa_mag} increases slightly when R_l increases. It is observed that the PA with


 Fig. 6. The load variation lines of Z_{in} for PA1 - PA3. (a) PA1. (b) PA2. (c) PA3.

 Fig. 7. The output power P_0 , the efficiency, the peak value of drain voltage V_{DS_peak} , and the magnitude of output current I_{pa_mag} for the CM Class-E PAs with different impedance transformation networks. (a) NC1. (b) NC2. (c) NC3.

larger C_S produce higher P_0 and V_{pa_mag} . The V_{DS_peak} decreases as R_l increases and stays under 90 V. All of them satisfy the targets we have set for the VM Class-E PA.

C. The Robustness of the output performance

The values of components in real circuits are usually not exactly the ones as designed and each component has a random error. Therefore, the network should be robust enough against these errors. The yield analysis is done to evaluate the robustness of the performance of the CM and the VM Class-E PAs. C_1 , C_2 and L_1 are subject to the Gaussian distribution and the deviation is set to be 5%. The efficiency over 90% at $R_l = 20 \Omega$ is considered to be qualified. 1000 samples are taken and the yield is defined as the ratio of the number of samples that satisfy the specification to the total number of samples 1000. According to the yield analysis in the simulation, the yield is 100% for these three CM Class-E PAs and the VM Class-E PA with $C_S = 330 pF$, 90% for the VM Class-E PA with $C_S = 215 pF$ and 61% for VM Class-E

PA with $C_S = 120 pF$. It is found that the performance of most CM and VM PAs are robust against the random errors, while the performance of the VM Class-E PA with small C_S is sensitive to the variation of components' value. Fig. 10 shows the load variation lines for Z_{in} of the network $NV1$ when L_1 deviates of $\pm 5\%$. They diverge a lot from the original one, resulting in degenerative output performance of PA.

The problem of sensitivity to random errors for the VM Class-E PAs with small C_S can be solved by slightly modifying the Π network. The topology of modified network is shown in Fig. 11 and the value of each component can be derived from the method same to that for the Π network. Note that the number of variables becomes four and the expression of Z_{in} should change. To validate the feasibility of this modified network, $NV1 - M$ is built for the VM Class-E PA with $C_S = 120 pF$ and compared with $NV1$. The parameter for each component in $NV1 - M$ is $C_{r1} = 2185 pF$, $C_{r2} = 1536 pF$, $L_{r1} = 527 nH$ and $L_{r2} = 816 nH$. The impedance response of $NV1 - M$ is close to that of the

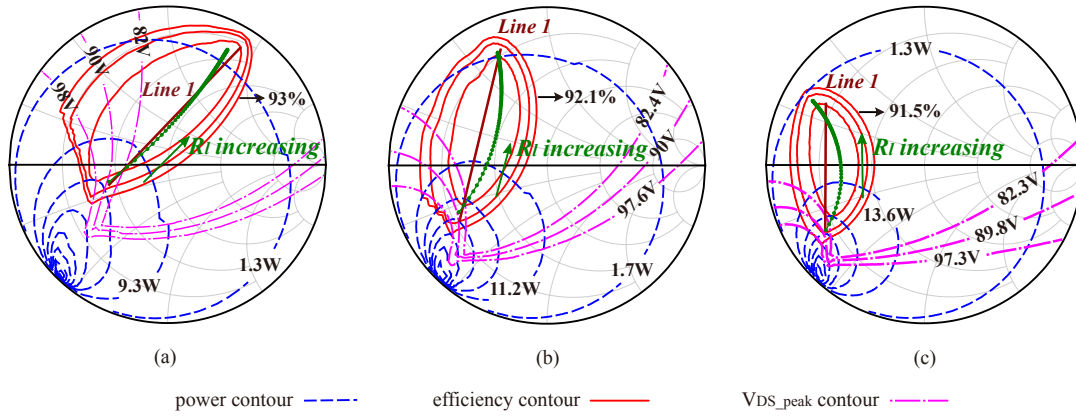


Fig. 8. The load variation lines of Z_{in} for PA1 - PA3. (a) PA1. (b) PA2. (c) PA3.

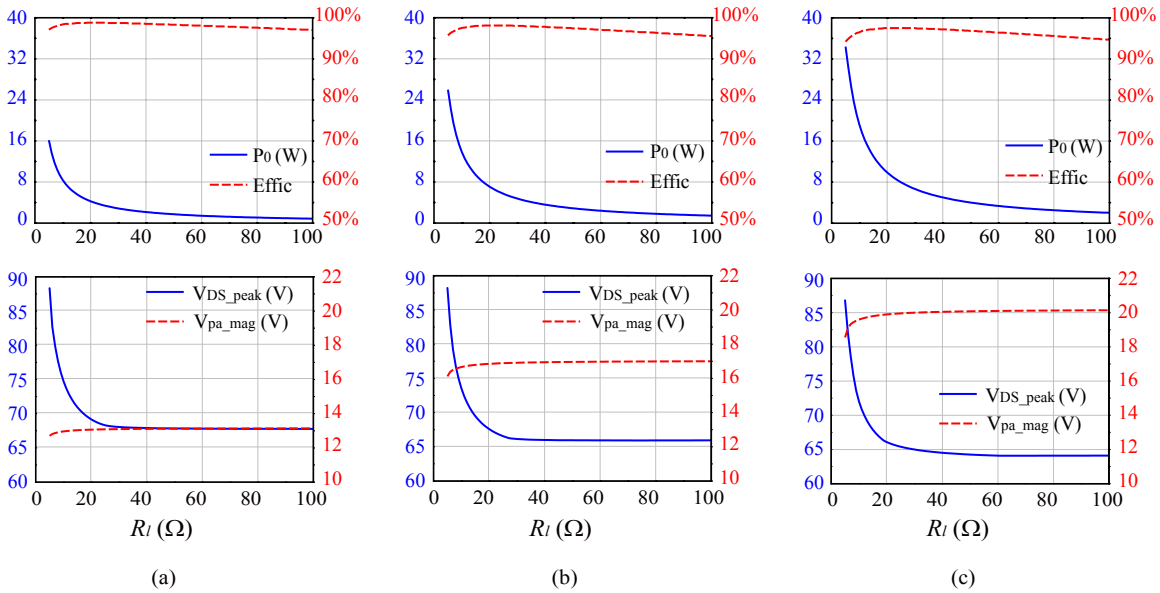


Fig. 9. The output power P_0 , the efficiency, the peak value of drain voltage V_{DS_peak} , and the magnitude of output voltage V_{pa_mag} for the VM Class-E PAs with different impedance transformation networks. (a) NV1. (b) NV2. (c) NV3.

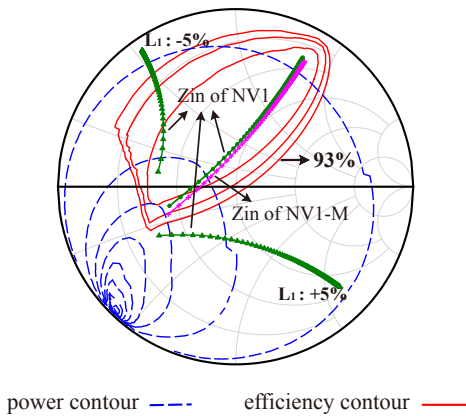


Fig. 10. The Z_{in} of NV1 and NV1-M when R_l is swept from 5 to 100 Ω .

network NV1, as is displayed in Fig. 10, while its performance is much more robust. Do the same yield analysis for the VM Class-E PA with NV1 - M and the yield turns out to be

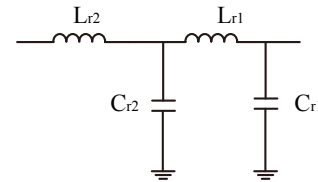


Fig. 11. The topology of the modified impedance transformation network.

100%.

IV. EXPERIMENTS

For verification purposes, a classical Class-E PA and two impedance transformation networks, $Net1$ and $Net2$, are designed and fabricated in house, as shown in Fig. 12. The CM Class-E PA is achieved by connecting $Net1$ with the classical PA, and the VM Class-E PA is achieved by connecting $Net2$ with the classical PA. Note that in WPT systems, the power source (PA or inverter) is usually expected to work as either

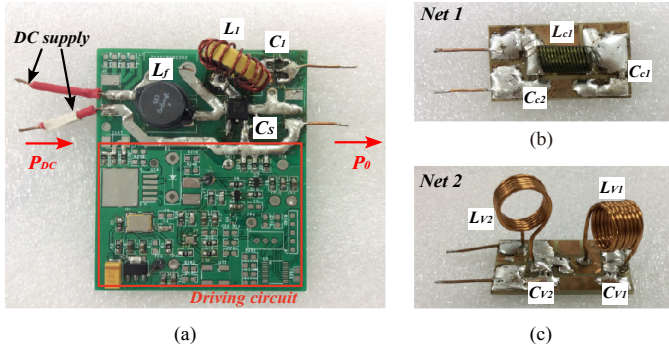


Fig. 12. The configurations of circuits made in house. (a) The classical Class-E PA. (b) The impedance transformation network *Net1* for the CM PA. (c) The impedance transformation network *Net2* for the VM PA.

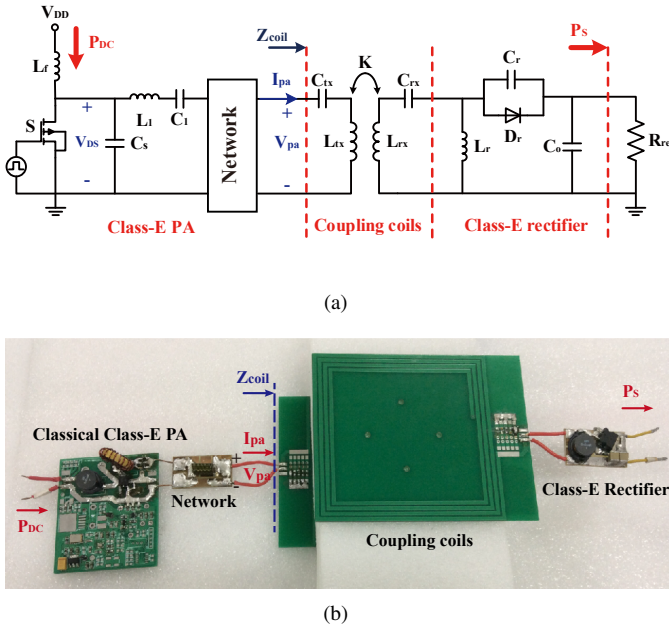


Fig. 13. The Experimental 6.78 MHz WPT system. (a) Schematic. (b) Photo.

a current source or voltage source (refer to [18], [19]). The three Class-E PAs, classical, CM, and VM ones, are tested and measured in a 6.78 MHz WPT system (see Fig. 13). The WPT system consists of a PA, coupling coils, and a Class-E rectifier. The SUD06N10 (MOSFET) and STPSC406D (Diode) are used as switches in the PA and the rectifier, respectively. The circuit specifications of the experimental WPT system are listed in Table IV. A 25 V V_{DD} is supplied to the WPT system. The load of PA is provided by the input impedance of the coupling coils Z_{coil} . The coupling coils and the rectifier are carefully designed so that Z_{coil} keeps approximately resistive. The coupling coefficient K changes from 0.088 - 0.3 by altering the distance between coils from 2 - 6 cm. The load of the rectifier is provided by an electronic load with a constant load 30 Ω . The Z_{coil} is calculated through the method described in [15] and it is found that Z_{coil} ranges from about 10 to 100 Ω . The output power of this WPT system is P_S (refer to Fig. 13) and the efficiency for the WPT system is defined as the ratio of P_S and P_{DC} .

The output performance of the WPT system with the

classical, the CM and the VM Class-E PAs is shown in Fig. 14. The efficiency of the WPT system with the classical Class-E PA improves as the coupling gets stronger and then drops when K continually increases. The output power has a similar trend versus K . The efficiency for the WPT system with the CM/VM Class-E PAs keeps high over 65% when K varies and the output power P_S increases/decreases monotonically with the increment of K . A small efficiency reduction is shown in Fig. 14(c) when K is large. It is caused by the deterioration of rectifier with small input power. Even through, there is a significant improvement compared to the WPT system with the classical Class-E PA.

The experimental waveforms of the three PAs (the drain voltages V_{DS} of the switch S) under different Z_{coil} are shown in Fig. 15. It can be seen that V_{DS} in the CM and VM Class-E PAs approach zero at the end of the OFF state, namely the soft switching. On the contrary, the drain voltage in the classical Class-E PA is high at the end of the OFF state when Z_{coil} largely deviates from its high-efficiency region, i.e., 50 or 100 Ω here. This indicates a large switching loss. The output performance of these PAs as a function of Z_{coil} is shown in Fig. 16. The output power of PA is obtained by taking the mean value of the product of V_{pa} and I_{pa} . The efficiency of the classical Class-E keeps high in a narrow range and drops quickly, and the output power increases as Z_{coil} increases at first and then reduces. For the CM Class-E PA, the efficiency stays over 87% when Z_{coil} ranges from 10 to 100 Ω and its P_0 is proportional to Z_{coil} . The magnitude of output current is almost constant, indicating that it operates as a current source. For the VM Class-E PA, the efficiency maintains above 83% and its P_0 is inversely proportional to Z_{coil} . The efficiency decreasing of the VM PA at high Z_{coil} is caused by the deterioration of the rectifier with small input power, which results in an increment of Z_{coil} 's reactance. Note that the efficiency can be pulled back over 90% if the V_{DD} is set to be 30 V. The magnitude of output voltage of this VM Class-E PA is almost constant, indicating that it works as a voltage source. The V_{DS_peak} for both CM and VM Class-E PAs is limited below 90 V, which ensures the safety of PA. The experiment results prove that the CM and the VM Class-E PAs designed through the proposed design methodology are high qualified and promising in WPT systems.

V. CONCLUSION

Class-E PA is a good option to act as the power source in high-frequency WPT systems, for its high efficiency and simple topology. However, it is sensitive to the load variation and it can neither work as a current source nor a voltage source. Therefore, conventional Class-E PAs are not qualified enough to adapt to real WPT applications. Here, two new types of high-efficiency Class-E PA for WPT systems are proposed and the design methodology for them is presented detailedly. The CM/VM Class-E PA is able to deliver increasing/decreasing power with increasing load and the efficiency of them maintains high even when the load varies in a large range. The design methodology makes full use of load-pull and impedance transformation techniques. An impedance

TABLE IV
CIRCUIT SPECIFICATIONS OF EXPERIMENTAL WPT SYSTEM.

Class-E PA	Net1	Net2	Coupling Coils	Class-E Rectifier
L_f 10 μH	C_{C1} 550 pF	C_{V1} 1366 pF	L_{tx} 3.24 μH	L_r 68 μH
C_S 220 pF	L_{C1} 520 nH	L_{V1} 590 nH	C_{tx} 165 pF	C_r 200 pF
L_1 3.27 μH	C_{C2} 390 pF	C_{V2} 1746 pF	L_{rx} 3.24 μH	C_o 44 μF
C_1 200 pF		L_{V2} 277 nH	C_{rx} 195 pF	

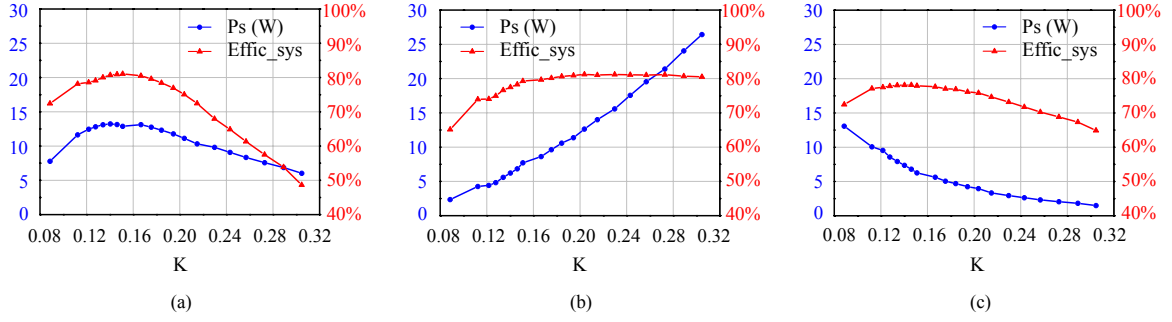


Fig. 14. The output performance of the WPT system with different PAs. (a) The classical Class-E PA. (b) The CM Class-E PA. (c) The VM Class-E PA.

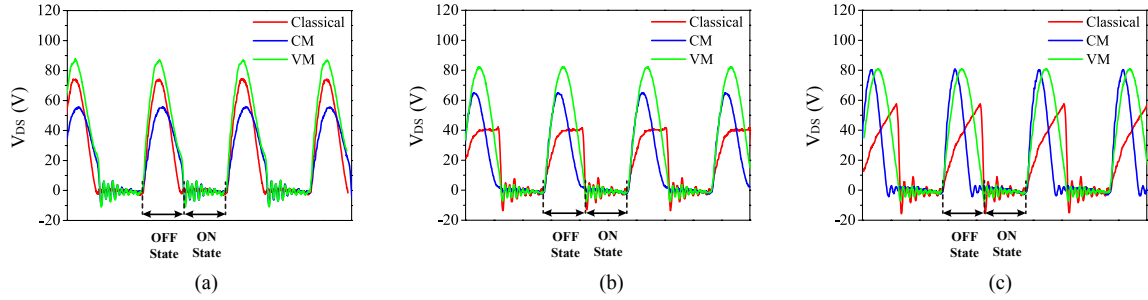


Fig. 15. The drain voltages V_{DS} of PAs under different Z_{coil} . (a) $Z_{coil}=10 \Omega$. (b) $Z_{coil}=50 \Omega$. (c) $Z_{coil}=100 \Omega$.

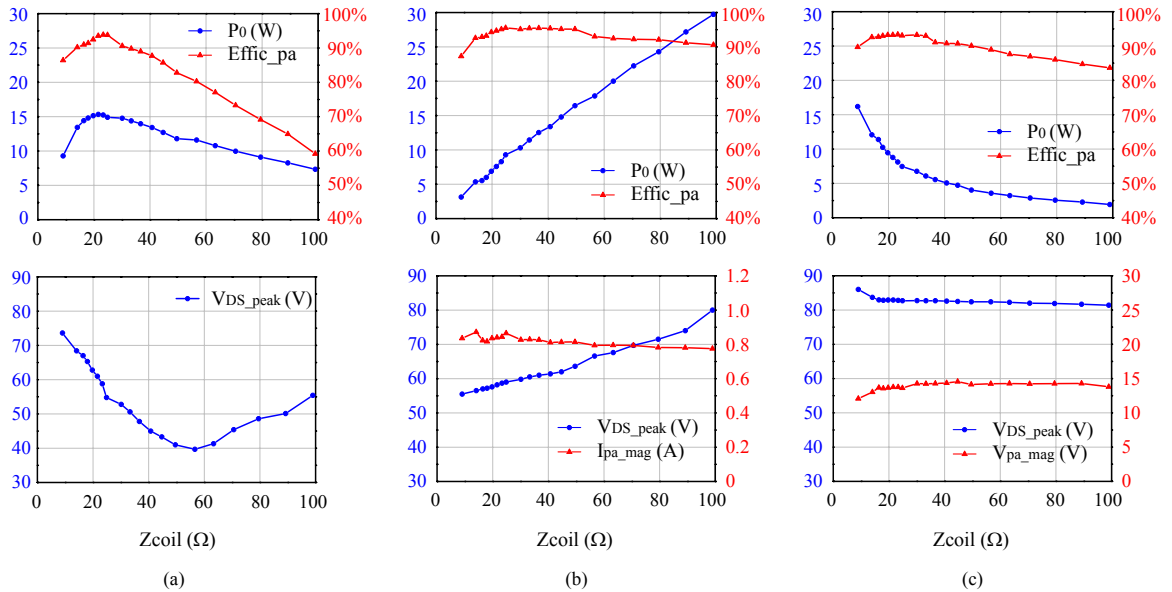


Fig. 16. The output performance of the Class-E PAs. (a) The classical Class-E PA. (b) The CM Class-E PA. (c) The VM Class-E PA.

transformation network is added into the circuit and transforms the loads of PA to targeted values. The efficiency, the output power, and the circuit tolerance are all taken into consideration in the process of designing the network, as well as the robustness against the component's random error, making the CM and the VM PAs high efficient and safe. Finally, the high-efficiency CM and VM Class-E PAs are fabricated and compared with the classical Class-E PA. The experiment results prove the validity of this design methodology and the performance of the CM and the VM Class-E PAs are much ahead of the classical one. It is believed that the CM and the VM Class-E PAs are promising to high-performance WPT systems.

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