A Low-Cost Voltage Equalizer Based on Wireless Power Transfer and Voltage Multiplier

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***Abstract*—This paper develops a novel voltage equalizer by combining wireless power transfer (WPT) and voltage multiplier (VM) for series-connected energy storage cells. The physical isolation achieved by WPT can offer several unique benefits that traditional equalizers can hardly provide. In this paper, the characteristics of a multiple-output VM are analytically discussed and used to develop an equivalent one-output VM model. Based on this model, parameters of the WPT system are properly designed. The proposed design methodology can achieve a single-switch voltage equalizer without feedback control, which dramatically decreases the circuit complexity and cost. Moreover, this methodology can naturally ensure a robust system under small coil misalignment. In the experiment, the proposed system is built to balance four series-connected ultracapacitor modules. The system efficiency is 72.8% at a load power level of 10 W.**

***Index Terms*—Voltage equalizer, low cost, wireless power transfer, voltage multiplier, robust design, single switch, Class E power amplifier.**

I. Introduction

ENERGY storage cells, such as batteries and ultracapacitors (UCs), are usually connected in series to meet the voltage requirements of specific applications. However, the parameter variance of individual cell can cause voltage imbalance, and lead to overcharging or over-discharging of individual cells [1]. To address this issue, various voltage equalization techniques have recently been developed. Dissipative equalizers can balance cell voltages by transforming excessive energy into heat, but this is obviously an unattractive solution [2]. In order to improve the efficiency, various non dissipative active equalizers have been developed. Examples of such efforts include dc/dc converters [3]–[7], switched capacitors [8], [9], and transformer-based converters [10], [11]. These techniques have the common issues in terms of the circuit complexity. Usually the number of active switches is proportional to the number of cells, which dramatically increases the complexity when more cells are in series [12]. Considering the drivers of active switches, high circuit complexity also indicates the cost and the size problem. Using a multiple-winding transformer can dramatically reduce the number of switches [10], [13]. The voltage equalization performance highly depends on the circuit parameter uniformity (such as the leakage inductance). It is a challenging issue for the multiple-winding transformer [2]. Another voltage-equalization scheme that reduces the number of switches is the use of voltage multipliers(VM). Additional switches (one or two) are added to control the overall energy. Both isolated and non-isolated VM-based voltage equalizer have been proposed [14], [15]. They have shown automatic voltage balancing ability with simple circuit structure.

In order to develop a low-cost and simple solution, a single-switch voltage equalizer is proposed by combining the wireless power transfer (WPT) and the VM. WPT can be viewed as a special power conversion technique and has been applied to charge wearable devices, cellphones, household appliances, and even electric vehicles [16]–[18]. The real physical isolation achieved by the WPT can provide several unique advantages that traditional equalizers can hardly offer. For example, the system works at weak coupling without magnetic cores, which leads to a low-profile receiver [16]. This receiver can be equipped with the charging cell in an enclosed design, and then the transmitter can be placed outside to improve safety. Additionally, the placement of the transmitter and the receiver are flexible, and they can be placed vertically or horizontally to achieve similar coupling [19], [20]. Moreover, if the cells do not need to be balanced all the time, different receivers are able to share the same transmitter to further save cost, because the transmitter is movable. Using WPT concept, the resonant coils will not suffer from the strict parameter matching issue. Because the self inductance is designed to resonate at the switching frequency [21]. The combination of existing voltage equalization techniques and wireless power transfer can bring more attractive features for the future energy-management system. This paper serves as the first trial to apply WPT in a single-switch VM-based voltage equalizer.

The proposed system consists of a Class E power amplifier (PA), two coupling coils, and a multiple-output voltage multiplier [refer to Fig. 1]. A 6.78 MHz system is built to increase the spatial freedom and reduce the coil size. The single-switch PA is used because of the simple circuit and high efficiency under zero voltage switching (ZVS) at high frequency [22]–[24]. The whole system works as a resonant converter, and

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the VM can naturally achieve zero current switching (ZCS). A one-output VM model is built to simplify the parameter design, and the VM input resistance is derived for the first time when the VM works as a part of a resonant converter. Based on the input resistance, a systematic design methodology is developed to optimize the parameters of the PA and the coupling coils. In this paper, the coupling coils are represented by their lump elements [25]–[27]. This coil model is straightforward and thus convenient for the following overall system design. The circuit parameters (including the coils and PA) are then optimized. The parameter design enables high-efficiency automatic voltage equalization without feedback control, which further simplifies the operation of the system. The design also enhances the robustness of the system performance against coil misalignment, i.e., coupling variations. The proposed system configuration and design methodology are helpful to build a WPT-based simple and low-cost voltage equalizer.

II. WPT System Driven Voltage Multiplier

A. Circuit Model of VM

Fig. 1 shows the system configuration. The VM is driven by a WPT system, which includes a single-switch Class E PA and the the coupling coils. The coils should be compensated based on the loading condition. Since the output voltage of the receiving coil is clamped by the final dc output, only series compensation can be applied to the receiving coil. The series compensation is also used for the transmitting coil because it can eliminate the reactance seen by the PA under a varied loading condition. To ensure high efficiency without feedback control, it is important to derive the input resistance of the VM under a voltage balancing process. The voltage multiplier has been used for voltage equalization in [14], [15]. These VMs are driven by PWM converters and have different characteristics under different driving circuits. In this paper, the whole system is a resonant converter. Although the VM circuit is not new and its working mechanism with sinusoidal input current has been discussed, the input resistance of the VM during a voltage balancing process has not been derived before. This input resistance, as a load of the WPT system, is important for parameter design to achieve high overall efficiency.

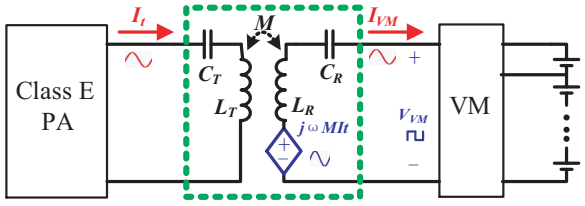


Fig. 1. Simplified system configuration.

In Fig. 1, two coils L_T and L_R are coupled through the mutual inductance M. The self-inductance is used for resonance, i.e., $j\omega L_T + 1/(j\omega C_T) = 0$ and $j\omega L_R + 1/(j\omega C_R) = 0$. The primary current ($I_t$) induces a voltage source at the secondary side, i.e., $j\omega M I_t$. Given the load, the power transfer capability among the coils is determined by this induced voltage. A higher frequency means a smaller M, which equally means smaller coil size and larger transfer distance. By increasing the switching frequency to several MHz, a compact WPT system with large spatial freedom becomes applicable. At this frequency band, 6.78 MHz is used because of the limited industrial-scientific-medical band [28]. At the secondary side, V_{VM} is a square waveform and I_{VM} is determined by the secondary resonant tank. If the high quality factor cannot be maintained, the VM will work under a distorted I_{VM} [29]. In this paper, the high quality factor is ensured by the high frequency. Therefore, the VM input current is sinusoidal, $I_{VM} = I_{MAG}\sin(\omega t)$, where I_{MAG} is the current magnitude.

A general n $\times$ voltage multiplier is shown in Fig. 2. This VM consists of n coupling capacitors (C_1 – C_n), 2n diodes ($D_{A,1}$ – $D_{A,n}$ and $D_{B,1}$ – $D_{B,n}$), n output filters ($C_{F,1}$ – $C_{F,n}$), and n series connected modules (B_1 – B_n, batteries or ultracapacitors). I_{VM} and V_{VM} are the input current and voltage. Through this paper, i is always used to denote different modules. $I_{C,i}$, $I_{DA,i}$, $I_{DB,i}$, and I_i are the currents of C_i, $D_{A,i}$, $D_{B,i}$, and B_i; $V_{C,i}$, $V_{DA,i}$, $V_{DB,i}$, and V_i are the voltages of C_i, $D_{A,i}$, $D_{B,i}$, and B_i. For each module B_i, there is a corresponding charging path consisting of C_i, $D_{A,i}$, $D_{B,i}$, and $C_{F,i}$. The overall output voltage is V_O.

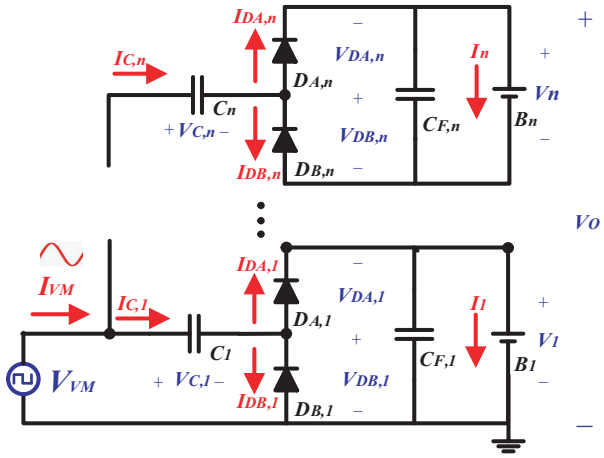


Fig. 2. WPT system driven voltage multiplier.

B. One-Output VM Model

Under a voltage balanced condition (i.e., $V_i = V_O/n$), the overall input current I_{VM} should equally flow into each charging paths (i.e., $I_{C,i} = I_{VM}/n$). The theoretical waveforms are shown in Fig. 3. $D_{A,i}$'s and $D_{B,i}$'s can conduct the current from C_i alternatively according to the polarity of I_{VM}. ZCS is achieved for all diodes. Due to the symmetry, the following discussion focuses on the positive cycle, i.e., $I_{VM} > 0$.

Since high resonance frequency (6.78 MHz) is used, the voltage ripple of $V_{C,i}$ is small and can be neglected. C_i serves as a DC block and its voltage equals to

$$V_{C,i} = -\sum_{m=1}^{i} V_m + 0.5V_i. \quad (1)$$

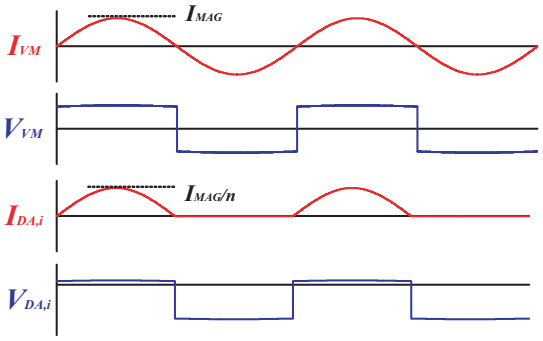


Fig. 3. Theoretical waveforms under a voltage balanced condition.

Applying Kirchhoff's Voltage Law (KVL) for each charging path gives

$$V_{VM} = I_{C,i}R_D + V_D + 0.5V_i,\ I_{C,i} \geq 0, \tag{2}$$

where R_D and V_D are the equivalent series resistance (ESR) and forward voltage of the diodes. Since

$$I_{VM} = \sum_{i=1}^{n} I_{C,i} \text{ and } V_O = \sum_{i=1}^{n} V_i, \tag{3}$$

adding up (2) for all charging paths gives

$$V_{VM} = \frac{R_D}{n}I_{VM} + V_D + \frac{1}{2n}V_O,\ I_{C,i} \geq 0. \tag{4}$$

Comparing (4) with (2), it shows the n-output VM can be equally represented by a one-output VM model. In this model, the diode forward voltage is still V_D. Its equivalent ESR R_{EQ}(=R_D/n) and output voltage V_{EQ} (=V_O/n) decrease by n times as shown in Fig. 4. Note that R_{EQ} is moved to be series with the input coupling capacitor without changing the diode conduction losses. And the ESR of C_i can also be absorbed by R_{EQ}. This model clearly shows that more charging paths are activated the less the VM conduction losses.

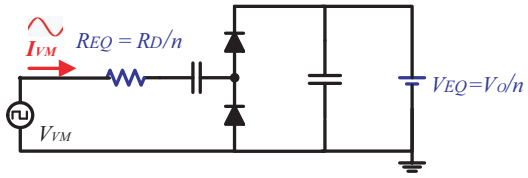


Fig. 4. Equivalent one-output VM model under a voltage balanced condition.

Under an imbalanced condition, I_{VM} is not equally distributed. A two-output VM serves as an example for discussion. In this two-output VM, it has

$$V_{MIN} \leq V_1 \leq V_2 \leq V_{MAX}, \tag{5}$$

where V_{MIN} and V_{MAX} are the minimum and maximum cell voltages. These voltage limits are usually defined by real applications. Note that the system characteristics are exactly the same if $V_2 \leq V_1$. Assume that both charging paths can be activated. According to (2), the current difference between $I_{C,1}$ and $I_{C,2}$ can be derived as

$$I_{C,1} - I_{C,2} = \frac{V_2 - V_1}{2R_D}. \tag{6}$$

Combining this equation with $I_{C,1} + I_{C,2} = I_{VM}$, $I_{C,1}$ and $I_{C,2}$ can be solved as

$$\begin{cases} I_{C,1} = \frac{I_{VM}}{2} + \frac{V_2 - V_1}{4R_D} \\ I_{C,2} = \frac{I_{VM}}{2} - \frac{V_2 - V_1}{4R_D} \end{cases}. \tag{7}$$

Since $V_2 \geq V_1$, it must have $I_{C,1} \geq I_{C,2}$ and Path 1 is activated. Then Path 2 is activated only if

$$I_{C,2} > 0 \Rightarrow 2I_{VM}R_D > V_2 - V_1. \tag{8}$$

Using I_{MAG} in this equation, it can determine whether Path 2 is activated during a switching cycle.

Fig. 5 defines two modes for this VM in a switching cycle. At Mode 1, only Path 1 is activated and all I_{VM} flows into C_1. With the increased I_{VM}, (8) is satisfied at certain time instant, leading to a current flowing into Path 2. This charging condition is defined as Mode 2. Then the current difference is determined by (6). It means the larger the voltage difference the larger the current difference will be. The VM can automatically balance the module voltage. All the diodes can still achieve ZCS under the imbalanced condition.

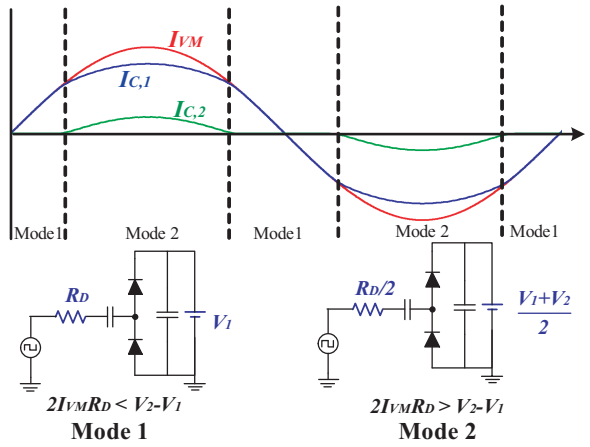


Fig. 5. VM modes when both paths are activated in a cycle (Status 2).

It is desirable to apply a one-output VM model for the imbalanced case by using equivalent ESR R_{EQ} and output voltage V_{EQ} [refer to Fig. 4]. When the initial voltage difference is large, (8) cannot be satisfied during a whole switching cycle, i.e., $2I_{MAG}R_D < V_2 - V_1$. Then an imbalanced system would experience three statues to become balanced. Under Status 1, the initial voltage difference is large and only Mode 1 exists during a cycle. It leads to an increasing V_1 and unchanged V_2. It has $R_{EQ} = R_D$ and $V_{EQ} = V_1$. With the increasing V_1, the VM goes into Status 2 once (8) is satisfied. Then both Mode 1 and Mode 2 coexist in a cycle as shown in Fig. 5. More currents flow into Path 1 to balance the voltage. Although it is difficult to exactly derive R_{EQ} and V_{EQ} for Status 2, the range of R_{EQ} and V_{EQ} can be obtained from Fig. 5, i.e., $R_D/2 \leq R_{EQ} \leq R_D$, and $V_1 \leq V_{EQ} \leq (V_1 + V_2)/2$. Finally, the voltage is balanced under Status 3. Only Mode 2 exists, and it has $R_{EQ} = R_D/2$ and $V_{EQ} = (V_1 + V_2)/2$. Therefore, R_{EQ} decreases and V_{EQ} increases during the voltage balancing process. Since

$V_1, V_2 \in [V_{MIN}, V_{MAX}]$, the variation ranges of R_{EQ} and V_{EQ} for this two-output VM are

$$\begin{cases} \frac{R_D}{2} \le R_{EQ} \le R_D \\ V_{MIN} \le V_{EQ} \le V_{MAX}. \end{cases} \quad (9)$$

In a n-output VM, an example case can be defined as

$$V_{MIN} \le V_1 \le V_2 \le \cdots \le V_n \le V_{MAX}. \quad (10)$$

Although there are infinite output voltage sequences under a voltage imbalance condition, the balancing mechanism is exactly the same, and the VM overall characteristics (such as the efficiency and the input resistance) do not change. There are at most n modes during a switching cycle. When multiple modes coexist, it is ineffective to derive the exact R_{EQ} and V_{EQ} during a dynamic balancing process. However, the variation ranges of R_{EQ} and V_{EQ} can be determined like the two-output VM, i.e.,

$$\begin{cases} \frac{R_D}{n} \le R_{EQ} \le R_D \\ V_{MIN} \le V_{EQ} \le V_{MAX} \end{cases}. \quad (11)$$

This boundary can be used to estimate the performance variation range of a n-output VM.

C. Efficiency and Input Resistance of the VM

The proposed one-output model is used to estimate the VM efficiency and input resistance. In a whole switching cycle, the output power is

$$P_O = \frac{1}{2\pi} \int_0^{\pi} I_{VM} V_{EQ} dwt. \quad (12)$$

The power loss due to diodes is

$$P_{LOSS} = \frac{1}{\pi} \left(\int_0^{\pi} I_{VM}^2 R_{EQ} d\omega t + \int_0^{\pi} I_{VM} V_D d\omega t \right). \quad (13)$$

The overall input power of the VM is

$$P_{VM} = P_O + P_{LOSS}. \quad (14)$$

Finally, the efficiency of the VM is derived as

$$\eta_{VM} = \frac{P_O}{P_{VM}} = \frac{2V_{EQ}}{\pi I_{MAG} R_{EQ} + 4V_D + 2V_{EQ}}, \quad (15)$$

and its input resistance is

$$R_{VM} = \frac{2P_{VM}}{I_{MAG}^2} = R_{EQ} + \frac{4V_D}{\pi I_{MAG}} + \frac{2V_{EQ}}{\pi I_{MAG}}. \quad (16)$$

These results show both η_{VM} and R_{VM} are dependent on V_{EQ} and R_{EQ}. Although it is ineffective to exactly calculate R_{EQ} and V_{EQ} during a dynamic voltage balancing process, (11) can be used to estimate the performance variation range of the VM.

A 4-output VM is used as an example to explain the overall characteristics. The diode is DFLS230L with $V_D = 0.42V$ and $R_D = 43m\Omega$ (used in the final experiment). Based on (12)-(15), Fig. 6 shows η_{VM} under different P_O. When $P_O = 5W$, the areas between by the black solid line ($R_{EQ} = R_D$) and the black dash line ($R_{EQ} = R_D/4$) shows the variation range of η_{VM} when $V_{EQ} \in [3V, 15V]$. In a typical balancing process, V_{EQ} increases while R_{EQ} decreases within the defined range [refer to (11)]. The decreasing R_{EQ} can explain the increasing η_{VM} during the balancing process. In the same manner, the areas defined by the blue lines and the red lines represent the variation range of η_{VM} when $P_O = 10W$ and $P_O = 15W$, respectively. It shows the larger the output power the smaller the efficiency. Therefore, in terms of efficiency, the voltage multiplier is not suitable for low-voltage modules that require high power.

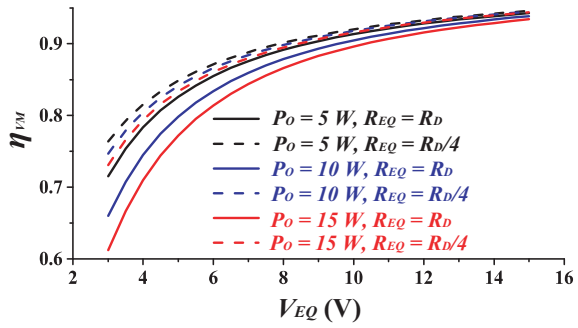


Fig. 6. The efficiency of a 4-output VM under different P_O.

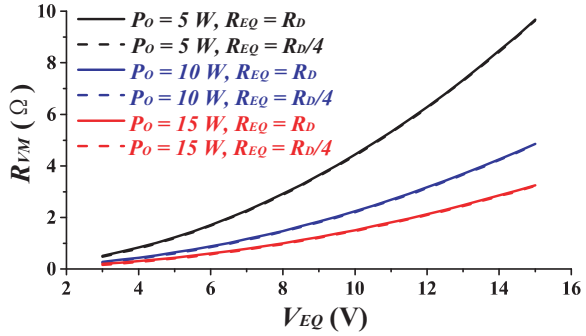


Fig. 7. The input resistance of a 4-output VM under different P_O.

Since the VM is driven by the WPT system, its input resistance is important for the parameter design of the driving circuit. Fig. 7 shows the variation range of R_{VM} for different P_O. It is interesting to note that R_{EQ} has limited influences on R_{VM}. Because the small R_{EQ} ($\le R_D$) can be equally viewed as a series component, which is only a small portion of R_{VM} [refer to (16)]. For a fixed V_{EQ}, higher the output power smaller the input resistance will be. Meanwhile, R_{VM} gradually increases with V_{EQ} during the voltage balancing process.

III. Design of the WPT System

A. System Configuration

The proposed WPT-based equalizer consists of a Class E power amplifier, two coupling coils, and a voltage multiplier as shown in Fig. 8. The PA and the coupling coils serve to drive the VM, which is represented by its one-output model. P_{PA} and P_{TX} are the input power of the PA and the coupling coils. The overall system efficiency is

$$\eta_{SYS} = \frac{P_O}{P_{PA}} = \eta_{PA} \cdot \eta_{COIL} \cdot \eta_{VM}, \quad (17)$$

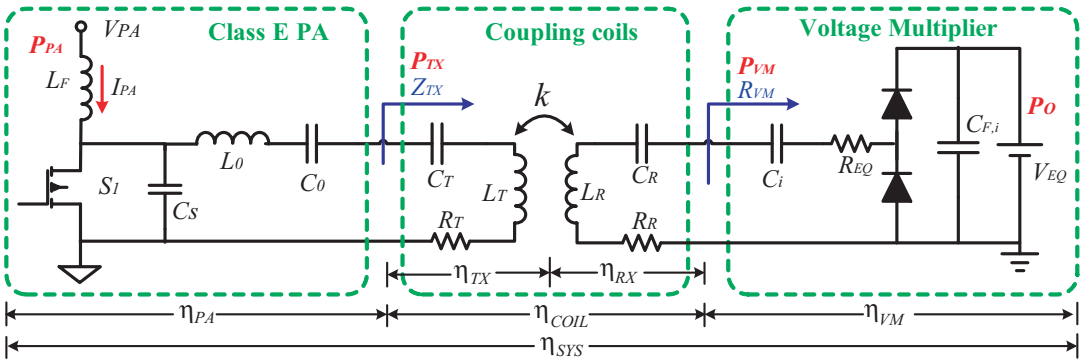


Fig. 8. System configuration.

where η_{PA} and η_{COIL} are the efficiency of the PA and the coupling coils. where η_{PA} and η_{COIL} are the efficiency of the PA and the coupling coils. Note that the objectives of the system parameter design may be different in various applications. For example, the WPT systems for bio-medical applications should pay special attention to specific absorption rate (SAR) and H-field to lower the risks of overheating and tissue damange [30], while the industrial WPT systems usually emphasize the system efficiency and the aspects of cost and complexity [26], [27], [31]. Considering the target industrial application of the voltage equalizers, the parameters are designed below to maintain high overall efficiency. The voltage balancing is a dynamic process. V_{EQ} increases within $[V_{MIN}, V_{MAX}]$. During this process, the loading condition (i.e., R_{VM}) seen by the WPT system changes and may significantly affect η_{PA} and η_{COIL}, namely the load sensitivity. Thus the parameters of the PA and coupling coils need to be designed and optimized to ensure robustness of the system under a varied loading condition.

B. Coupling Coils

It is the weak-coupling coils that can achieve real physical isolation, which the strong-coupling transformer can hardly offer. The avoidance of the iron core also eliminates the risks of core damage and the consequent overheating and short circuit problems. Besides, the whole system can be easily implemented with PCB boards, and thus the parameter variance is small. As shown in Fig. 8, the constant self-inductance is used to achieve resonance, i.e., $j\omega L_T + 1/(j\omega C_T) = 0$ and $j\omega L_R + 1/(j\omega C_R) = 0$. This is quite different to the transformer-based resonant converter using leakage inductance for resonance, which may suffer from the fabrication variance. The weak coupling is represented by the coupling coefficient k. The quality factors of L_T and L_R are

$$Q_T = \omega L_T / R_T, \text{ and } Q_R = \omega L_R / R_R, \tag{18}$$

where R_T and R_R are the ESR of the coupling coils.

Under resonance, the input impedance of the coupling coils is

$$Z_{TX} = R_T + \frac{\omega^2 k^2 L_T L_R}{R_R + R_{VM}}. \tag{19}$$

The coil efficiency consists of two parts, the efficiency of the transmitting coil η_{TX} and the efficiency of the receiving coil η_{RX} [refer to Fig. 8]. According to the power division law, it has

$$\left[\begin{cases} \eta_{COIL}=P_{VM}/P_{TX} = \eta_{TX}\eta_{RX} \\ \eta_{TX}=(Z_{TX}-R_T)/Z_{TX} \\ \eta_{RX}=R_{VM}/(R_{VM}+R_R) \end{cases}\right. . \tag{20}$$

A basic trend of η_{COIL} is shown in Fig. 9. With the increasing R_{VM}, η_{RX} increases and η_{TX} decreases, which leads to a parabola η_{COIL}. An efficiency peak exists to maximize η_{COIL}, and this peak value can be derived as

$$\frac{d\eta_{COIL}}{R_{VM}} = 0 \Rightarrow R_{VM,P} = \frac{\omega L_R}{Q_R}\sqrt{Q_T Q_R k^2 + 1}. \tag{21}$$

In order to fully utilize the peak η_{COIL}, it should ensure that $R_{VM,P}$ can appear during the voltage balancing process, i.e., within the variation range of R_{VM} [refer to Fig. 9]. Note that the objective here is not ensure the coils always work at its maximum efficiency. Instead it should guarantee the coils work around the peak η_{COIL} to achieve high η_{SYS}. This objective is achieved by the parameter design.

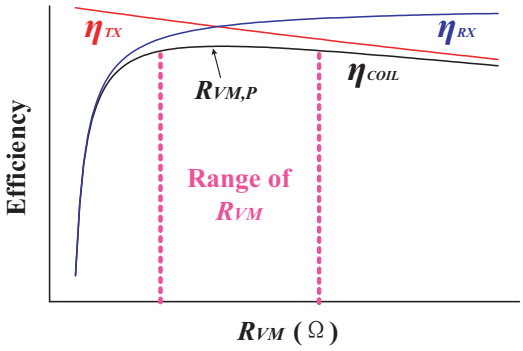


Fig. 9. Efficiency of the coupling coils.

In practice, the planar receiver can be placed to the side surface of the charging module. For a specific application, the coil shape and size should be designed based on its own requirements. Usually, a rectangular coil is preferred because it can fully use the surface area. This paper uses a rectangular coil as shown in Fig. 10. A two-layer printed circuit board (PCB) can be used to implement a spiral coil with different numbers of turns. Here the litz wire is not used because the PCB coil has much higher parameter uniformity and is much easier for mass production. Besides, the benefit of using litz

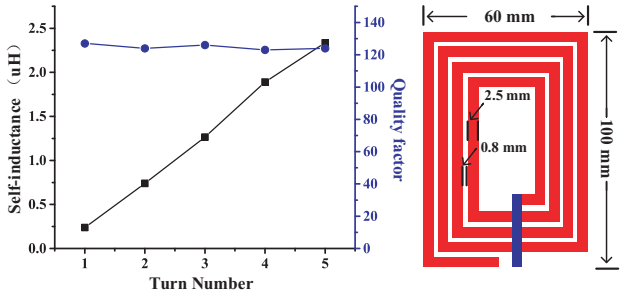


Fig. 10. The coil parameters with different turn number (N).

wire is limited in the MHz frequency range due to the need to have strand diameters much smaller than the skin depth [32]. With the selected coil shape, the Ansys Maxwell is used to estimate the self-inductance and quality factor. The inductance is almost proportional to the turn number N instead of N^2. This is because the resonance frequency (6.78 MHz here) is close to the self-resonance frequency of the PCB coil, and the linear inductance model used at low frequency is no longer valid. As a result, it is interesting to find that the quality factor is almost a constant. Another important parameter is the coupling coefficient k. For example, when a receiver is enclosed with the charging module in a case, the transmitter is placed outside the case. Then the distance should be at least larger than the case thickness. Once the distance is defined by the application, the coupling coefficient can be measured.

Based on above information, the receiving coil can be designed. First of all, L_R is roughly estimated to ensure that $R_{VM,P}$ is located within the range of R_{VM}. Using Fig. 7 as an example, a 10 W VM has a varied R_{VM} from 0.2 Ω to 5 Ω when V_{EQ} increases from 3V to 15V. Then $R_{VM,P}$ is desired to be located within [0.2 Ω,5 Ω]. A suitable range of L_R is calculated based on (21). Then the turn number of L_R can be determined according to Fig. 10. It is interesting to find that $R_{VM,P}$ only depends on L_R and is not affected by L_T. L_T actually provides the design freedom for the PA, and will be discussed later.

C. Class E PA

A Class E PA driven WPT system is proposed in [21], and the feedback-based control is used to optimize the efficiency under load and coupling variation. This paper use the same circuit configuration for the PA and the coupling coils. However, the targeting load is a VM with varied output voltage under a relatively fixed coupling. Note that small coil misalignment (k variation) is allowable and will be discussed later. A low-cost solution is proposed by using no controllers. Thus a well-performed system is highly dependent on a system-level optimization, which is not discussed in [21].

As shown in Fig. 8, the classical PA consists of a switch S, a radio frequency choke L_F, a shunt capacitor C_S, and a series resonant tank L_0C_0. V_{PA}, I_{PA}, and P_{PA} are the input voltage, current, and power of the PA. The input impedance of the coupling coils, Z_{TX}, serves as the load of the PA. For a target load Z_{OPT}, the circuit parameters are optimized under any operating frequency ω using Raab's equations,

$$\begin{cases} B = \omega C_s = \frac{8}{\pi(\pi^2+4)Z_{OPT}} \approx \frac{0.184}{Z_{OPT}} \\ X = \omega L_0 - \frac{1}{\omega C_0} = \frac{\pi(\pi^2-4)}{16} Z_{OPT} \approx 1.15 Z_{OPT} \end{cases}, \quad (22)$$

where B is the susceptance of C_s [33]. It means Z_{OPT} determines C_S, L_0, and C_0. The detail analytical model has been discussed in [21], and only the power-efficiency characteristics are reviewed here. According to [21], PA's output power P_{TX} and efficiency η_{PA} can be analytically derived for any Z_{TX} and V_{PA}, i.e.,

$$\begin{cases} P_{TX} = f(Z_{TX}, V_{PA}) \\ \eta_{PA} = g(Z_{TX}) \end{cases}. \quad (23)$$

It means P_{TX} is affected by Z_{TX} and V_{PA}, and η_{PA} is only affected by Z_{TX}. Using normalized parameters (V_{PA}=1 V and Z_{OPT} = 1 Ω), Fig. 11 shows η_{PA} and P_{TX} under different Z_{TX}. It shows high η_{PA} is achievable within an impedance region around Z_{OPT}. This parabola η_{PA} means the design consideration for η_{COIL} can be applied here. The circuit parameter should be designed to ensure that Z_{OPT} is located within the variation range of Z_{TX} [refer to (19)]. Thus the high peak efficiency of PA is fully utilized during the voltage balancing process. Following is the design procedure.

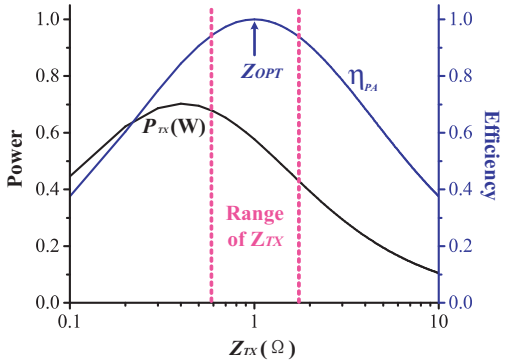


Fig. 11. Efficiency and output power of PA.

- Step 1: Choose the input voltage. For example, if S_1 is a 100 V MOSFET, V_{PA} should be smaller than 28V (=100V/3.6), because the voltage rating of S_1 is about $3.6V_{PA}$ at the optimal point. Consider the safety margin, 20V input voltage can be used.
- Step 2: Calculate Z_{OPT} according to V_{PA} and target output power. For a given Z_{OPT}, since C_S, L_0, and C_0 are optimized according to (22) and V_{PA} is known in Step 1, a figure such as Fig.11 can be obtained. Note Fig.11 is plotted with V_{PA}=1 V and Z_{OPT} = 1 Ω. Sweeping Z_{OPT}, find the one that $P_{TX}(Z_{OPT})$ equals to the target power (such as 10W).
- Step 3: In (19), the range of R_{VM}, k, and L_R are known, and each L_T gives a varied Z_{TX} within a specific range. Find a proper L_T in Fig. 10 such that Z_{OPT} is located within the range of Z_{TX}.

D. Parameter Design and Optimization Methodology

The proposed methodology fully utilizes the peaks of η_{COIL} and η_{PA} during a voltage balancing process. Thus high η_{SYS} is achieved without using feedback control. The design flow chart is shown in Fig. 12. Given the system specifications, the performance of VM is estimated to obtain the range of R_{VM}. Then this range is used to design the receiving coil (L_R) for high η_{COIL}. Meanwhile, Z_{OPT} is designed based on the target power level (P_{TX}) and input voltage (V_{PA}). The circuit parameters of PA (C_S, L_0, and C_0) can then be optimized toward Z_{OPT}. Finally, L_T is designed to maintain high η_{PA}.

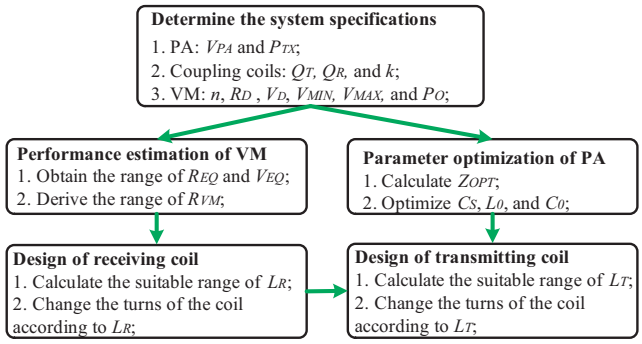


Fig. 12. Design flow chart.

During the voltage balancing process, the varied R_{EQ} affects η_{VM} while it has limited influence on R_{VM} [refer to Fig.6 and Fig. 7]. Since the parameters of PA and coupling coils are designed according to R_{VM}, a voltage balanced condition is sufficient to justify the validity of the proposed design methodology. A 4-output system is designed (used in the experiment), and the system parameters are given in Table I. Using the analytical model, Fig. 13 shows the efficiencies of all the circuits. It shows that both the peaks of η_{PA} and η_{COIL} appear when V_{EQ} increases from V_{MIN} to V_{MAX}, and high average η_{SYS} is achieved.

As discussed in the introduction, the physical isolation achieved by the WPT technique provides several unique advantages, such as low-profile receivers, enclosed design, sharing the transmitter, and flexible placement. In some cases, small coil misalignment may happen and it may affect the system performance, because the parameters are designed for a fixed coupling case. However, this influence is limited because the proposed methodology is naturally robust under small coupling variation (i.e., coil misalignment). Recall that the idea is to utilize the peaks of η_{PA} and η_{COIL} during the dynamic balancing process. So the parameters are optimized for a varied load instead of a fixed one. For the transmitter, a varied coupling can be viewed as a kind of varied load. Therefore, the system designed under a fixed coupling can naturally be robust under small coupling variation. For example, a fixed k leads to a known peak η_{COIL} in Fig. 13. Then the varied k can make the peak η_{COIL} shift either to the left or right. If the variation is small, the peak η_{COIL} will still occur during the balancing process. Similar conclusion can be applied for the PA. Therefore, high η_{SYS} is still achievable. This is another benefit of the proposed methodology.

TABLE I
SYSTEM PARAMETERS

PA	**Freq.**	$\boldsymbol{S_1}$	$\boldsymbol{V_{PA}}$	$\boldsymbol{L_F}$
	6.78 MHz	SUD06N10	20 V	10 μH
	$\boldsymbol{C_S}$	$\boldsymbol{L_0}$	$\boldsymbol{C_0}$	$\boldsymbol{Z_{OPT}}$
	431 pF	2.41 μH	258 pF	10 Ω
Coils	$\boldsymbol{k}$	$\boldsymbol{L_T}$	$\boldsymbol{Q_T}$	$\boldsymbol{C_T}$
	0.1	1.89 μH (4 turns)	124	291 pF
	Size	$\boldsymbol{L_R}$	$\boldsymbol{Q_R}$	$\boldsymbol{C_R}$
	10cm $\times$ 6cm	0.24 μH (1 turn)	127	2.3 nF
VM	$\boldsymbol{n}$	$\boldsymbol{V_{MIN}}$	$\boldsymbol{V_{MAX}}$	$\boldsymbol{P_O}$
	4	2 V	10 V	10 W
	$\boldsymbol{V_D}$	$\boldsymbol{R_D}$	$\boldsymbol{C_i}$	$\boldsymbol{C_{F,i}}$
	0.42 V	43 mΩ	1 μF	1 μF

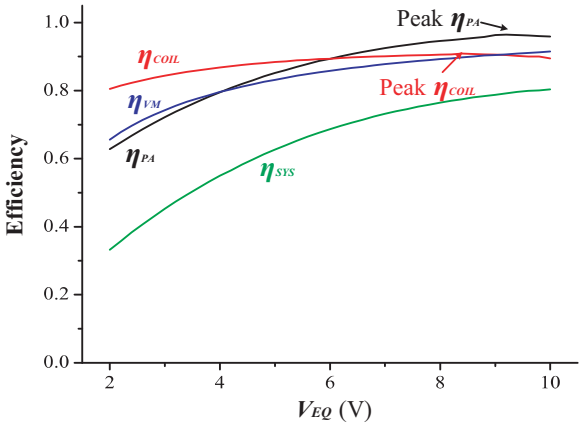


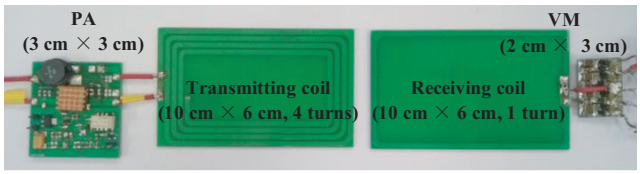
Fig. 13. Efficiency of different power stages under a voltage-balanced condition.

IV. Experimental Verification

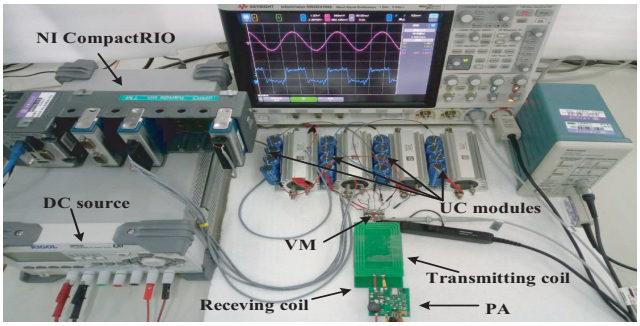
A. Experiment Setup

A WPT-based voltage equalizer is built according to Table I. As shown in Fig. 14 (a), this voltage equalizer consists of a 6.78 MHz PA, a transmitting coil, a receiving coil, and a 4-output VM. Fig. 14 (b) shows the measurement platform. In the PA, the 6.78 MHz signal from an on-board crystal is amplified by the driver (LM5114) and then used to drive the switch (SUD06N10). The gate driving loss is also included in the measured efficiency. Four series-connected UC modules (25 F) are balanced. The wide output voltage range (2–10 V) can help to justify the potential applications of the proposed equalizer. Both the input and output voltage and current (i.e., V_{PA}, I_{PA}, V_i, and I_i) are measured by a NI CompactRIO controller. During the balancing process, the input voltage is fixed at the designed value, i.e., $V_{PA} = 20$ V, and no feedback is used for power control purposes. As shown in Fig. 8, in the real circuit C_0 and C_T can be merged into a single capacitor, but C_R and C_i cannot be merged. Because each charging path needs a dc block.

The prototype system shows that the receiver (receiving coil and VM) is small and planar. No magnetic core is required to boost the coupling. During the experiment, the coils are placed face to face (i.e., 100% overlap) with a 2 cm vertical distance ($k = 0.1$). This large distance is sufficient for the receiver to be equipped with the charging modules in an enclosed design.



(a)



(b)

Fig. 14. Experiment setup. (a) WPT-based voltage equalizer. (b) Measurement platform.

Note that the placement is flexible. The coils can also be placed horizontally side by side to achieve similar coupling. This large spatial freedom is due to the use of high resonance frequency.

B. Voltage Balanced Condition

The voltage equalizer is first used to charge four UC modules under a voltage balanced condition. At the initial state, the voltage of each UC module is 2 V. The overall efficiency η_{SYS} is recorded under different V_{EQ} as shown in Fig. 15. The calculated η_{SYS} is compared with the measured η_{SYS} without misalignment (i.e., 100% overlap). They are well matched with each other. When V_{EQ} is small, the parasitic resistors of components (such as S_1, L_F, L_0, and UC modules) will become more obvious, leading to a larger error between calculation and experiment. Although the system parameters are optimized for a fixed coupling case (i.e., the 100% overlap), the system performance is robust under small coupling variation. The dash line in Fig. 15 shows the efficiency for an 80% overlap case, and small misalignment has very limited influence on η_{SYS} as the analysis predicts. Finally, the input current and voltage of the VM are shown in Fig. 16. These waveforms are consistent with the theoretical waveforms in Fig.3. ZCS is achieved for the diodes. Because of the high frequency (6.78 MHz), a square V_{VM} with ringing is observed because of the resonance between the lead inductance and junction capacitance of the diode.

C. Voltage Imbalanced Condition

A voltage imbalanced system is tested with different initial voltages, i.e., 2V, 4V, 6V, and 8V. The charging profile are shown in Fig. 17(a) and (b). At the beginning, B_1, B_2, and B_3 are charged with different currents. B_1 with the lowest voltage has the largest charging current. The current distribution automatically changes in a manner to balance the

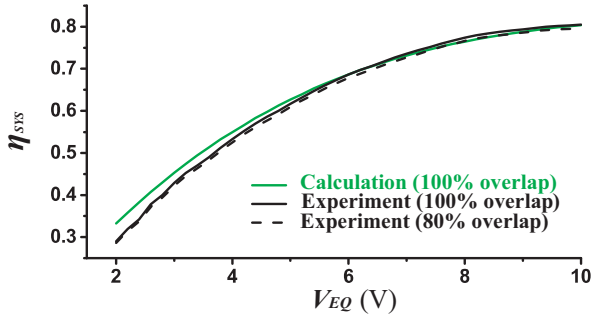


Fig. 15. Efficiency comparison.

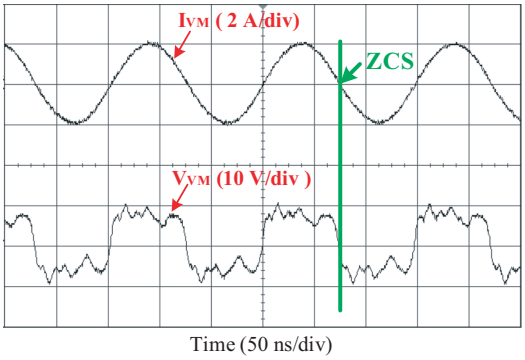
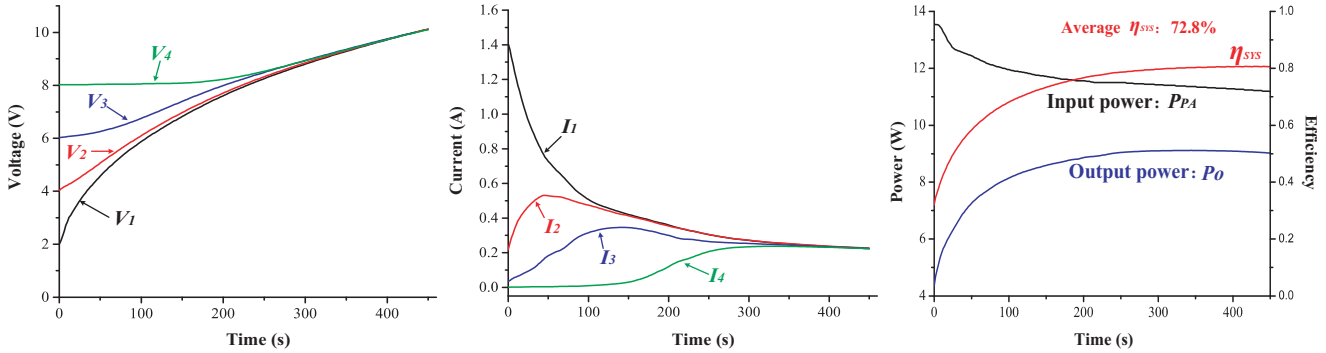


Fig. 16. Measured VM input current and voltage.

voltage at different time. Finally, a voltage-balanced condition is achieved at 350 s. The modules are charged under a voltage balanced condition and the input current is equally distributed among all modules.

The power and efficiency are shown in Fig. 17(c). The overall system efficiency η_{SYS} increases and tends to be stable after 250 s. During the whole charging period (from 0 to 450 s), the average η_{SYS} is 72.8%, and no feedback is used for power control purposes. Therefore, both P_{PA} and P_O change with time. The stable value of P_O is about 9 W, which is different from the design target 10 W. This is because the system parameters are all designed based on the analytical model, in which the component parasitic resistances of the PA and the UCs are not considered. So the real output power P_O is smaller than the target one. This error can be compensated by choosing the input voltage V_{PA} larger than the designed value (20 V). Usually, larger output power leads to smaller balancing time but lower efficiency. Therefore, there is a trade-off between balancing time and efficiency. In this paper, a 10 W system is built, which shows to be a good compromise. It is attractive for the medium- and low-power applications.

Table II compares the system complexity and performance of different voltage equalizers. By using dc/dc converters, the voltage equalizer can achieve high controllability and high efficiency. However, the number of active switches and inductors are usually proportional to the number of cells [3]–[6]. By using multiple-winding transformers or switched capacitors, no inductors are required in [8], [9], [11]. But the circuit is still very complicated. The VM can dramatically reduce the number of active switches, which make it very attractive



(a) (b) (c)

Fig. 17. System dynamic response during a voltage balancing process. (a) The voltage of the UC modules. (b) The charging current of the UC modules. (c) System input power, output power, and overall efficiency.

TABLE II
COMPLEXITY AND PERFORMANCE COMPARISON OF DIFFERENT VOLTAGE EQUALIZERS

Ref.	Topology	Active switch	Inductor	Capacitor	Diode	Cell voltage (V)	Efficiency	CHG Power/cell (W)
[3]	DC-DC converter	n+1	n+1	1	n+1	13-14.5	N/A	28
[4]	DC-DC converter	2(n-1)	2(n-1)	n-1	0	3.2-4	N/A	N/A
[6]	DC-DC converter	n	n-1	0	0	3.2-4	80%-85%	5-20
[5]	DC-DC converter	2(n-1)	2(n-1)	n-1	0	3-4	80%	4
[7]	DC-DC converter	2n+1	0	2	1	2-2.5	60%	2
[8]	Swiched capacitor	2n	0	2n-3	0	3.2-4	N/A	N/A
[9]	Swiched capacitor	2n	0	1	0	2.6-3.3	76%-92%	0.2-1.8
[11]	Transformer-based	n	0	0	0	2.6-3.3	71%-86%	0.3-2.6
[10]	Transformer-based	2	0	0	n+2	10-13.6	N/A	N/A
[15]	Transformer-VM-based	1	0	n+2	2n+1	8-15	85%	5
[14]	VM-based	1	1	n	2n	8-15	80%-87%	6
This paper	WPT-VM-based	1	2	n+4	2n	2-10	72.80%	2

for low-cost equalizers. The VM-based equalizers have shown good efficiency at high output voltage (8-15V) [14], [15]. Besides the circuit complexity and efficiency, another important system objective is the time of the whole balancing process, namely a criterion in time responses. For the same application, the larger charging power per cell, the shorter balancing time will be. As shown in the last column of Table II, the proposed system can achieve similar power level compared to most of the existing systems. Overall, this paper proposes a WPT system to drive the VM, and then a physically isolated system becomes possible. This attractive feature particularly enables an enclosed design of the receiver to improve safety.

V. CONCLUSION

In this paper, a single-switch multiple-output voltage equalizer is proposed for series-connected energy storage cells. Through the new combination of wireless power transfer and voltage multiplier, the source and the cells are physically isolated in the voltage equalizer. In order to accurately evaluate the VM performance, an equivalent one-output VM model is developed for the multiple-output VM, and then variation range of efficiency and input resistance are investigated using the VM model. Based on the VM characteristics, a systematic design methodology is proposed to ensure high overall efficiency without the need of controlling the input power. The system configuration and design methodology provide a simple and low-cost solution for the equalization of the cell voltages.

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